

## Remarks

Applicants respectfully request that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicants submit that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicants believe that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Applicants acknowledge the allowance of claims 35-38 and 40. Further, applicants acknowledge that claims 12, 22, 28, 34 and 39 would be allowable if rewritten to include the features of the base claim and any intervening claims.

Claims 1, 5, 8, 9, 23, 28, 29, 41, 42, 44 and 45 have been amended. No claims have been canceled. Therefore, claims 1, 3, 5, 7-25, 27-38, 42, 44, 45 and 47 are now presented for examination.

Claims 1, 3, 5, 7, 9-11, 14, 17-18, 21, 23-25, 27, 32-33, 41-42, 44-45, and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger et al. (U.S. Pub. No. 2003/0135694) and Auerbach et al. (U.S. Patent No. 6,199,126). In addition, claims 15-16, 30-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger and Auerbach. Applicants submit that the present claims are patentable over Naffziger in view of Auerbach.

Naffziger discloses a compression engine for a cache memory subsystem that has a pointer into cache tag memory and cache data memory and an interface coupled to the pointer and capable of being coupled to cache tag memory, and cache data memory. The interface reads tag information and uncompressed data from the cache and writes modified tag information and compressed data to the cache. The compression engine also has compression logic for generating compressed data and generating compression successful information, and tag line update circuitry for generating modified tag

information according to the compression successful information and the tag information.  
See Naffziger at Abstract.

Auerbach discloses an apparatus and method for transparent on-the-fly decompression of the program instruction stream of a processor. A decompression device is connected between a processor and a memory storing compressed information. The decompression device, receives a request from the processor for information, retrieves compressed information from the memory, decompresses the retrieved compressed information to form uncompressed information, and transmits the uncompressed information to the processor. The compressed information may include both program instructions and data. When the decompression device receives a request for information, which includes an unmodified address, from the processor, it generates an index offset from the received unmodified address. An indexed address corresponding to the generated index offset is retrieved from an index table. Compressed information corresponding to the selected indexed address is retrieved from the memory and transmitted to the processor. See Auerbach at Abstract

Claim 1 of the present application recites a process wherein if a compression bit indicates a cache line is compressed a companion bit is disregarded and if the compression bit indicates the cache line is not compressed the companion bit is compared with a tag. Applicants submit that both Naffziger and Auerbach fail to disclose or suggest such a feature. Thus, any combination of Naffziger and Auerbach would also fail to disclose or suggest the feature. As a result claim 1 is patentable over Naffziger in view of Auerbach. Claims 3, 5 and 7-22 depend from claim 1 and include additional features. Thus, claim 3, 5 and 7-22 are also patentable over Naffziger in view of Auerbach.

Claims 23, 35 and 42 recite similar features described above with respect to claim 1. Accordingly, claims 23, 35 and 42 and their respective dependent claims are also patentable over Naffziger.

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger et al. and Auerbach et al and Yanai et al. (U.S. Patent No. 5,206,939). Applicants submit that the present claims are patentable over Naffziger and Auerbach even in view of Yanai.

Yanai discloses an apparatus and method for disk mapping and data retrieval includes a data storage medium on which has been stored a plurality of data records. See Yanai at Abstract. Nonetheless, Yanai does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger and Auerbach do not disclose or suggest such a feature. Thus, any combination of Naffziger, Auerbach and Yanai would also not disclose or suggest the feature. As a result, the present claims are patentable over Naffziger and Auerbach in view of Yanai.

Claim 13 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger et al. and Auerbach et al and Gross (U.S. Pub. No. 2004/0255209). Applicants submit that the present claims are patentable over Naffziger and Auerbach even in view of Gross.

Gross discloses an embedded memory on an integrated circuit has a memory cell array equipped with replacement cells and mapping logic for electronically substituting the replacement cells for defective cells at least one location in the memory cell array. The memory also has programmable links for storing redundancy information in a compressed format, and decoding logic for decompressing the redundancy information and controlling the mapping logic. See Gross at Abstract.

However, Gross does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger and Auerbach

do not disclose or suggest such a feature. Therefore, any combination of Naffziger, Auerbach and Gross would also not disclose or suggest the feature. Accordingly, the present claims are patentable over Naffziger and Auerbach in view of Gross.

Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger et al. and Auerbach et al and Wang et al. (U.S. Patent No. 6,507,895).

Applicants submit that the present claims are patentable over Naffziger and Auerbach even in view of Wang.

Wang discloses an apparatus for memory access demarcation. Nevertheless, Wang does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger and Auerbach do not disclose or suggest such a feature. Thus, any combination of Naffziger, Auerbach and Wang would also not disclose or suggest the feature. Consequently, the present claims are patentable over Naffziger and Auerbach in view of Wang.

Claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger et al. and Auerbach et al and Shimoi et al. (U.S. Patent No. 5,652,857).

Applicants submit that the present claims are patentable over Naffziger and Auerbach even in view of Shimoi.

Shimoi discloses logic blocks which were swept out from a non-compression cache memory that are compressed by a compressing circuit and combined to a compression group (logic sector size) of a fixed length in which a plurality of compression data are collected by a compression group forming unit. See Shimoi at Abstract. However, Shimoi does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above,

Naffziger and Auerbach do not disclose or suggest such a feature. Thus, any combination of Naffziger, Auerbach and Shimoi would also not disclose or suggest the feature. Therefore, the present claims are patentable over Naffziger and Auerbach in view of Shimoi.


Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,  
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